What is Claimed is:

1. An apparatus for inspecting errors in a system board including a number of channels for controlling the overall operation of a system, comprising:

means for judging signals respectively received in the number of channels of the system board;

means for comparing the signals respectively received in the number of channels of the system board to output signals respectively informing if the channels are failed or not; and

means for respectively transmitting normal signals to the failed channels, which are respectively inputted by said comparing means, to maintain the operation of the system board.

2. An apparatus for inspecting errors in a system board according to claim 1, wherein said judging means, comparing means and maintaining means are provided as the form of a single chip.

3. An apparatus for inspecting errors in a system board according to claim 1, wherein said judging means comprises:

a bypass terminal for separating a signal of the failed channel when interruption of the signal is required due to repair of the failed channel in the system board; and

a manual trip terminal capable of forcibly changing the output value of said judging means to convert the operation.

4. An apparatus for inspecting errors in a system board according to claim 1,

wherein said comparing means compares the input signals in the channels of the system board, and if a channel outputs a signal different from the other channels, outputs a signal informing that the channel outputting the different signal is failed.

5. An apparatus for inspecting errors in a system board according to claim 1, wherein said maintaining means comprises a logic circuit for transmitting an operation signal simultaneously with the signal outputted from the failed channel in the system board to normally maintain the operation of the system board upon receiving the failed channel informing signals.

6. An apparatus for inspecting errors in a system board according to claim 5, wherein said logic circuit is an OR gate.

7. A method of inspecting errors in a system board, comprising the following steps of:

receiving output signals in a voter from a number of channels of the system board;

receiving the output signals in a comparator simultaneously with the voter from the number of channels of the system board to compare the output signals;

comparing the output signals to output a signal informing that a channel outputting a signal different from the other channels is failed; and

transmitting and logic-combining a feedback signal simultaneously with the output signal of the failed channel to input a normal signal to the voter.